TECH 3232
End of Semester Project
Fall 2024

Ver 3.21

Background:

As discussed in class, a Finite-State Machine is a sequential circuit that will produce a sequence of outputs based upon its design.

In this project you will be assigned a sequence to generate (base on a sudo random number generator using the last 4 digits of your U number as the seed). You will then determine the circuit, using the method discussed in class and the provided excel spreadsheet, to determine the logic needed for the various J-K inputs. You will then simulate the circuit, draw a schematic, build the circuit, and create a demo video of the final circuit.

Procedure:

1. Goto http://tech-uofm.info/fsm/, type in the last 4 digits of your U number and submit. You will be given a random sequence of decimal numbers
2. Download the Excel Template for this project
3. Fill in the state diagram based on the values given above
4. Fill in the Present State / Next State table
5. Using the table (from step 4) and the Transition Table for a JK Flip-Flop (Provided), create the Karnaugh Maps for present-state J and K inputs for each of the flip flops (all unused location become “Don’t Cares”)
6. Show the groupings for the K-Maps (using Insert | Shapes with no fill) and derive and enter the minimized Boolean equation for each input (use equation editor to place the equation in the spaces provided in the excel spreadsheet)
7. Open SimcirJS via the Set and Get link (this will allow you to edit the text for the OSC (see hints). Also note that you must use the JK-FF Block – DO NOT use the JKFFPC or JKFFPCFE block! Lastly bring the outputs (Q’s) to a 4bit7seg block (so you can see the count)
8. Draw the circuit diagram in KiCad or similar schematic program.
9. Build the circuit
10. Test the circuit
11. Generate a video of the circuit in operation (Please make sure you state the sequence your counter is supposed to generate in the video).

Hints:

- Since all values in the sequence are 0-7, how many Flip-Flops will you need?
- Since it is synchronous counter, what does this tell you about the clk inputs of the JK FFs?

- If you use the OSC to generate the clock in your SimcirJS simulation, and it is going to quickly, get the text of the simulation and change the line like this:

  {"type":"OSC","id":"dev0","x":160,"y":408,"label":"OSC"}

  By adding the highlighted section (leave the rest of the text as is on your sim):

  {"type":"OSC","id":"dev0","x":160,"y":408,"label":"OSC","freq":1}
- Use the 555 timer circuit to clock your circuit (use the first set of resistor / cap values so the count will be slow enough to be viewed)
- Use the 7-seg driver to display the numbers in the sequence. (See Lecture Notes for Complex TTTL Devices, Slide 21 for an example circuit).
- It is recommended that you use 7473A IC's (note the 'A' does matter) as your J-K FF.. Since this IC has an unused $\overline{clr}$ pin, it will have to be set inactive for the counter to work. Also note this IC has unusual connections for Vcc and Gnd – make sure you check the datasheet!

NOTE: Instructor will NOT assist you in debugging your circuit unless a properly drawn schematic is available!

Submit (via class submission website):

- Excel Spreadsheet
- Text File containing code for SimcirJS simulation
- PDF Of full schematic
- Video link (in space provided in Excel spreadsheet) of the circuit demo