TECH 3232
Lab 9
Fall 2025

Ver 3.0

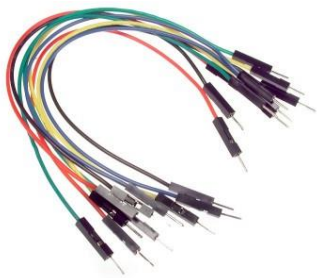
Objective - To design, build and **FULLY TEST** an Asynchronous 4 bit BCD Counter with a 7-segment display output.

Circuit MUST be designed using 7476A JK Flip Flops (no counter IC's allowed). Note that the 'A' at the end of the IC #. Unlike most IC's in the TTL Family, the 7476 and 7476A have a minor difference, the A works better for this lab.

You can test that your circuit is working correctly by using the 555 timer (use first setup from the 555 timer lab) or by using the function generator (see Function Generator handout linked on class website) and set the frequency to 2Hz (0.5 Sec).

Instructor and/or Lab assistant will NOT assist in debugging your circuit without a properly drawn, labeled, and numbered schematic diagram available!

Hook up the Rigol Digital Analyzer to your circuit (Channel 0 to the LSB, Channel 1, Channel 2, Channel 3 to MSB and Channel 4 to your Clear signal of your circuit) using the jumper wires as shown below:



To avoid damaging the Rigol Digital Analyzer cable). Load Lab9a.stp. Press the "SINGLE" button on the scope and wait for the Run/STOP button to turn red. Capture the image of the full count of your counter. Now load Lab9b.stp. Press the "Single" button again and wait for the Run/Stop button to turn red. Use the cursors to measure the time of the signal on channel 4. Capture the image (including the cursor data).

Demo to the instructor (and make sure it is recorded).

Create a document including your name and lab #, the two captures in order and the answer to the following question:

> *For Capture 1 – include a 2nd copy of the first image. Use paint to show the binary count by adding 1's and 0's to the digital analyzer output.*

For Capture 2 - Given the time measured on channel 4 in the second capture does the off time of this signal make sense? HINT: Look on the data sheet. Back up your answer with an explanation of the time and how it relates to what the data sheet is telling you.

Submit a full schematic drawn in KiCad and saved as a pdf (note: you can use a Place | NET PORT symbol for the 555 timer output from the 1st circuit from the previous lab as input to the 1st clock input, you do NOT have to draw the 555 timer circuit), and the document containing the required information via online submission.