

# TECH 3821

## ADC0804 Analog-to-Digital Converter

ver 2.4

Name: \_\_\_\_\_

Partner: \_\_\_\_\_

In this lab you'll use the ADC0804 chip, which is an eight-bit successive approximation A/D converter using CMOS technology.

Since the ADC0804 has an 8-bit output, how many different digital output codes can it produce?

If we use 5 V as its reference voltage ( $V_{REF}$ ), what is this ADC's step size? (The step size is the smallest analog input voltage that will produce a digital output code of \$01.) Since you'll be using this number in many calculations below, record it to three significant digits: don't round it off to one or two digits.

If we use 5 V as its reference voltage ( $V_{REF}$ ), what is this ADC's full-scale voltage? (This is the smallest analog input voltage that will produce a digital output code of \$FF.)

In a spreadsheet, Calculate the output of the ADC (in Decimal, Binary and Hex) given the inputs on the table below (format the spreadsheet similar to the table shown)

Input (V)	Predicted			Input (V) (measured)	Measured		
	Dec	Binary	Hex		Dec	Binary	Hex
0.1							
0.2							
0.5							
0.7							
1							
1.5							
2							
2.5							
3							
4							
4.5							
5							

You can use the functions `dec2bin()` and `dec2hex()` to calculate the binary and hex values (please keep 8 places in the binary conversion)

Show the results to the instructor BEFORE PROCEEDING)

Instructor Sign off

The ADC0804 is a versatile chip that can be configured in many different ways, depending on how its pins are connected to each other and to external components. In this lab you'll use the ADC0804 in a self-clocking mode by using an external RC timing network. The device is optimized for a clock around 600 kHz and requires approximately 64 clock cycles per conversion. The clock frequency may be figured by the following equation:

$$f_{CLK} = 1 / (1.1 * R * C)$$

Does this equation ring any bells? It should, since it is very similar to an equation that you used to calculate the timing of 555 multivibrator circuits, which also used external RC timing networks.

Conversions are initiated by pulsing the chip's  $\sim$ WR line (pin 3) low. The conversion cycle begins when this line goes high again.  $\sim$ WR must then remain high during the conversion or the process will be abandoned. When the conversion is complete the  $\sim$ INTR line (pin 5) produces a low pulse to indicate an end-of-conversion (EOC).

In this circuit we've tied  $\sim$ INTR and  $\sim$ WR together, so that as soon as one conversion is completed, another one is immediately begun. Differential analog voltage inputs allow offsetting the analog zero input voltage value. This means that the  $V_{in(-)}$  input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading. In addition, the  $V_{REF/2}$  input (pin 9) can be adjusted to allow converting a smaller analog voltage span to the full 8 bits of resolution. In this experiment, the  $V_{REF/2}$  input will be set at 2.5 volts. Therefore our reference voltage  $V_{REF}$  is equal to 5 V.



