TECH 3232
Final Lab Project
Fall 2018

V1.3

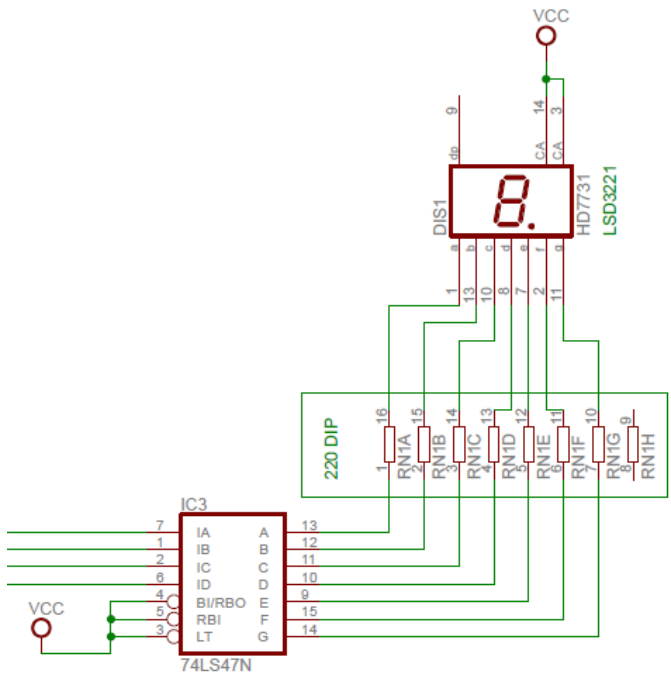
This project and report is worth 15% of your final grade in this class.

Objective - To design, build and **FULLY TEST** a 4 bit BCD Counter (asynchronous or synchronous is acceptable) with a 7-segment display output.

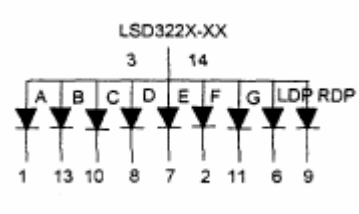
Circuit MUST be designed using JK Flip Flops (no counter IC's allowed) and can be either a synchronous or asynchronous design (tradeoff is that one is harder to build but has less glitches to analyze, the other is easier to build but has more glitches).

Since we have not used a 7-Seg Display Driver this semester….a little background on 7-Seg Driver (7447). This IC takes a BCD Input (marked 1D, 1C, 1B, 1A with 1A being the LSB) and outputs the proper on / off signals for segments A-G for a Common Anode 7-Seg Display.

Here is an example wiring for this part of the circuit:



7-Seg pinout



LSD3221 equivalent to 24740

Note: Even though pins are "missing" you still count the pins as if the pin is there:

Since we have a limited number of digital analyzers, you might have to test your circuit outside of lab time (arrange a time with the instructor to use the digital analyzer).

You can test that your circuit is working correctly by using the 555 timer (use first setup from the 555 timer lab) or by using the function generator (see Function Generator handout linked on class website) and set the frequency to 2Hz (0.5 Sec).

Instructor will NOT assist in debugging your circuit without a properly drawn, labeled and numbered schematic diagram available!

Once it is functional (ie counting correctly use the digital analyzer to collect the timing diagrams required for the report (see below).

Notes on Digital Analyzer:

The name and password for the Digital Analyzers are:

user1
la168xx

When the digital analyzer boots up select the "Final_Proj" Icon. This will load the setup file for this lab.

To test the circuit on the digital analyzer, set up the Function Generator as per handout (see link on class website) and set the frequency to 25KHz (note – at this speed it will look like your counter is stuck on the number 8….this is normal. Can your see something changing at 25KHz).

Connect the following:

Digital Analyzer	Your Circuit
Pod 1 – 0	Counter LSB
Pod 1 – 1	|
Pod 1 – 2	|
Pod 1 – 3	Counter MSB
Pod 1 – 4	Clock
Pod 1 – 5	Clear
Pod 1 – GND	GND

Refer to Lab #8 for more details.

Semi Formal **Lab Report and circuit demonstration due DEC 12, 2018 by 3pm** – NO EXCEPTIONS! Please submit the report on paper and via electronic submission.

Semi Formal lab report should include a proper schematic (drawn with Cadence, Eagle Cad or other professional grade schematic capture software), Digital Analyzer Output of the circuit (with Explanation) and analysis of any glitches/errors found during the testing phase. Background, procedure, parts list and conclusion **not required** (only results and discussion)